ABSTRACT

The frequency changes in a bang-bang PLL that are generated using a digital phase detector's up/down signal are initially set to produce a faster pull-in rate and then reduced to produce a slower pull-in rate. The faster pull-in involves relatively large frequency changes and the slower pull-in rate involves smaller frequency changes. The changes in frequency of a bang-bang PLL can be implemented using a step size controller that includes timing control logic and step size logic. The function of the timing control logic is to control the timing of step size changes. The function of the step size logic is to set the step size of the frequency changes that are made by the VCO in response to the pd_up/down signal that is delivered directly to the VCO from the digital phase detector.